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SH **Scott Hamilton**
scott.hamilton@atos.net
Jun 25 2024, 3:29 PM UTC

As requested by Akim Houari I have submitted a L3 bug on bugzilla. See it here:
https://bugzilla.suse.com/show_bug.cgi?id=1226962

DB **Daniel Blueman**
daniel@numascale.com
Jun 21 2024, 7:14 AM UTC

Hi Micah and related SuSE team,

We (Eviden and Numascale) are still awaiting your update on this ticket and kindly ask if there are any technical or non-technical issues, so we may understand what is holding up moving it forward.

Please note the fix has already been incorporated into Red Hat Enterprise Linux, as such we have this opportunity to ensure SuSE SLES doesn't carry any limitations on these MESCA5 (and as rebadged by other vendors) platforms.

Many thanks,
Daniel

SH **Scott Hamilton**
scott.hamilton@atos.net
Jun 11 2024, 3:49 PM UTC

Micah,
It has been a week since the escalation of this ticket and I still have not received any news. It is a simple ask, the patch has been accepted upstream and we just need to know when it will be integrated to the official SLES kernels.
Kind Regards,

Hello,

I apologize for the delayed response. I will get up to date and see what I need to do to assist with this issue.

Regards,

Micah Stone
Technical Support Engineer, SUSE Customer Support
SUSE Documentation | Knowledge Base
SUSE Technical Support Handbook

ref:!00D1i0gLOd.!500Tr07g8wT:ref

SS **SUSE Support**
techsupport@suse.com

Jun 5 2024, 3:10 PM UTC

Bryant Kettle
Support Manager, SUSE Customer Support
https://www.suse.com/support/kb/

ref:!00D1i0gLOd.!500Tr07g8wT:ref

SS **SUSE Support**
techsupport@suse.com

Jun 5 2024, 2:54 PM UTC

DB **Daniel Blueman**
daniel@numascale.com

May 20 2024, 10:02 PM UTC

Hi all, I am the author of the patch and BIOS/platform contractor for Eviden (Atos). It has been accepted in upstream already, and will be shipped with 6.10-rc1:

https://git.kernel.org/pub/scm/linux/kernel/git/tip/tip.git/commit/?id=455f9075f14484f358b3c1d6845b4a438de198a7

May we know the timeframe for it being backported by SuSE to the SLES and relevant products?

Thanks, Daniel

SH **Scott Hamilton**
scott.hamilton@atos.net

May 20 2024, 7:15 PM UTC

Scott Hamilton removed the following participant from the case:
productops@suse.com

SH **Scott Hamilton**
scott.hamilton@eviden.com

May 20 2024, 7:08 PM UTC

Daniel,

Sorry I was dealing with a power outage this morning. I just sent you an invite to the Atos group on Suse with access to support allowed. I am not 100% sure it will work with an e-mail outside the organization, but I gave it a shot.

Thanks,
Scott

Bull/Atos/Eviden group; I am a contractor for the same.

This prevents me updating this case [1]. Kindly assist giving Scott the code so he may pass onto me.

Thanks,
  Daniel

[1] You are not currently entitled to use the support system. You may need to enable it in your organization page. Please refer to our FAQ for more information.
--
Daniel J Blueman
Principal Software Engineer, Numascale

_____
From: SUSE Technical Support <techsupport@suse.com>
Sent: 17 May 2024 23:17
To: productops@suse.com; scott.hamilton@atos.net
Cc: akim.houari@suse.com; emeaorders@suse.com; scott.hamilton@eviden.com; Daniel J Blueman; christophe.ledorze@suse.com; micah.stone@suse.com; partnerteam.emea@suse.com; james.cleverdon.external@eviden.com
Subject: SUSE Support # 01415631: TSC clocksource spuriously declared invalid in 12+ socket Sapphire Rapids systems [ref:_00D1igLOd._500Tr7g8wT:ref]

Scott Hamilton posted a new message on the case:

Dear Team,

I am taking over the tracking of this ticket as James is no longer with Eviden. What I really need is for someone to acknowledge the high importance of this patch as it is critical in the performance of any multi-socket system over 4-sockets. It greatly impacts the overall performance of the system.

It would also really help if I could get some commitment on the timing of the patch release so we know what we can communicate with customers. We have not had an update on this particular ticket from your side since March 26.

If there is anyhing you need from us to move forward please reach out to me and I will do my best to provide the information.

Thanks,
Scott

Case: https://scc.suse.com/support/cases/01415631

--
Best Regards,
Product & Pricing Configuration Operations (PCO)
Please see our PCO Google Site with additional information that may answer your questions.

DJ **Daniel J Blueman**
daniel@numascale.com
May 18 2024, 3:48 AM UTC

DJ **Daniel J Blueman**
daniel@numascale.com
May 18 2024, 3:44 AM UTC

SH **Scott Hamilton**
scott.hamilton@atos.net
May 17 2024, 3:17 PM UTC

Dear Team,

I am taking over the tracking of this ticket as James is no longer with Eviden. What I really need is for someone to acknowledge the high importance of this patch as it is critical in the performance of any multi-socket system over 4-sockets. It greatly impacts the overall performance of the system.

It would also really help if I could get some commitment on the timing of the patch release so we know what we can communicate with customers. We have not had an update on this particular ticket from your side since March 26.

If there is anyhing you need from us to move forward please reach out to me and I will do my best to provide the information.

Thanks,
Scott

PS **ProductOps SUSE**
productops@suse.com
May 7 2024, 10:51 PM UTC

Can you please remove this email address from this case? I do not know how it was added, but we should not be included AFAIK.
Thank you,
Melonie

On Tue, May 7, 2024 at 9:36 AM SUSE Technical Support <techsupport@suse.com> wrote:

Reviewed-by: Steffen Persvold <sp@numascale.com>
Reviewed-by: James Cleverdon <james.cleverdon.external@eviden.com>
Reviewed-by: Dimitri Sivanich <sivanich@hpe.com>
Reviewed-by: Prarit Bhargava <prarit@redhat.com>
Link: https://eur06.safelinks.protection.outlook.com/?url=https%3A%2F%2Flore.kernel.org%2Fr%2F20240419085146.175665-1-daniel%40quora.org&data=05%7C02%7Cjames.cleverdon.external%40eviden.com%7Cffee17b03ed24ebda3e308dc6894a9cc%7C7d1c77852d8a437db8421ed5d8fbe00a%7C0%7C0%7C638500234906994997%7CUnknown%7CTWFpbGZsb3d8eyJWIjoiMC4wLjAwMDAiLCJQIjoiV2luMzIiLCJBTiI6Ik1haWwiLCJXVCI6Mn0%3D%7C0%7C%7C%7C&sdata=soqFmXakYQQNK5ZFKR66k2BkSDhAzCKFdxnxyEgkpiM%3D&reserved=0
---
arch/x86/kernel/tsc_sync.c | 6 ++----
1 file changed, 2 insertions(+), 4 deletions(-)

diff --git a/arch/x86/kernel/tsc_sync.c b/arch/x86/kernel/tsc_sync.c
index 1123ef3..4334033 100644
--- a/arch/x86/kernel/tsc_sync.c
+++ b/arch/x86/kernel/tsc_sync.c
@@ -193,11 +193,9 @@ bool tsc_store_and_check_tsc_adjust(bool bootcpu)
	cur->warned = false;

	/*
-	 * If a non-zero TSC value for socket 0 may be valid then the default
-	 * adjusted value cannot assumed to be zero either.
+	 * The default adjust value cannot be assumed to be zero on any socket.
	 */
-	if (tsc_async_resets)
-		cur->adjusted = bootval;
+	cur->adjusted = bootval;

	/*
	 * Check whether this CPU is the first in a package to come up. In

---

ProductOps SUSE <productops@suse.com> — May 2 2024, 2:40 PM UTC

The account is A145747. The support ticket Case 01415631 · TSC clocksource spuriously declared invalid in 12+ socket Sapphire Rapids systems (suse.com) is already in place with the Technical Support team. I do not see any update since April 9th from SUSE on this ticket, however.
I have copied techsupport on this thread along with Micah Stone from SUSE who is identified in the ticket.
ProductOps cannot assist any further with this issue. Please work with Tech Support or Micah for futher assistance.

Please add this patch to SLES 15.
Thank you!
James Cleverdon james.cleverdon.external@eviden.com Apr 29 2024, 2:11 AM UTC
Has there been any progress on the more specific patch I proposed?

It should only change how the MSR_IA32_TSC_ADJUST value is handled on systems that ask for it with "tsc=trust_adj_msr".

Thanks!

- Apr 19 2024, 4:53 PM UTC **James Cleverdon** james.cleverdon.external@eviden.com
  Daniel Blueman has posted a minor change to the patch. It is functionally identical:
  https://lore.kernel.org/lkml/20240419085146.175665-1-daniel@quora.org/T/

  Any progress on this issue?

  Thanks!

  Apr 9 2024, 12:57 AM UTC **James Cleverdon** james.cleverdon.external@eviden.com
  Hi Micah,

  Any news on this patch? (We're going to be selling these systems soon and would like to tell customers that the TSC fix is coming.)

  If your engineers feel that changing this for everyone is too invasive, maybe we could use a kernel cmdline parameter to set a flag to trust the value in the TSC adjust MSR, like the attached patch?
  trust_adj_msr_patch.diff (1.89 KB)

  Apr 9 2024, 12:49 AM UTC **James Cleverdon** james.cleverdon.external@eviden.com
  Hi Micah,

  Any news on this patch? (We're going to be selling these systems soon and would like to tell customers that the TSC fix is coming.)

  If your engineers feel that changing this for everyone is too invasive, maybe we could use a kernel cmdline parameter to set a flag to trust the value in the TSC adjust MSR, like the attached patch?

  (Sorry about compressing it, but Outlook changes the whitespace in an inline patch.)

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SUSE Technical Support Handbook

ref:!00D1i0gLOd.!500Tr07g8wT:ref

-

-

Mar 25 2024, 6:06 PM UTC **James Cleverdon** james.cleverdon.external@eviden.com
And here's Dan's original patch.
daniel_tsc_spinics_2024-02-26.patch (1.84 KB)

Mar 25 2024, 6:00 PM UTC **James Cleverdon** james.cleverdon.external@eviden.com
This minor variation on the patch might be better accepted upstream, since the kernel coding guidelines frown on multiple assignments per line.
x.diff (713 Bytes)

James Cleverdon
Technical Expert
E BDS INN R&D
Portland, Oregon, USA
1-208-860-5831
an atos business

--
Best Regards,
Product & Pricing Configuration Operations (PCO)
Please see our PCO Google Site with additional information that may answer your questions.

--
Best Regards,
Product & Pricing Configuration Operations (PCO)

Is there anything I can do to help move this fix forward?
Thanks!

James Cleverdon
james.cleverdon.external@eviden.com

Apr 22 2024, 3:26 PM UTC

Anything new either on Dan's patch, or the more specific one I proposed?
Thanks!

James Cleverdon
james.cleverdon.external@eviden.com

Apr 19 2024, 4:53 PM UTC

James Cleverdon added new participants to the case:
daniel@numascale.com
They will receive email notifications on any new case activity.

James Cleverdon
james.cleverdon.external@eviden.com

Apr 19 2024, 4:53 PM UTC

Daniel Blueman has posted a minor change to the patch. It is functionally identical:
https://lore.kernel.org/lkml/20240419085146.175665-1-daniel@quora.org/T/

Any progress on this issue?

Thanks!

James Cleverdon
james.cleverdon.external@eviden.com

Apr 9 2024, 12:57 AM UTC

Hi Micah,

Any news on this patch? (We're going to be selling these systems soon and would like to tell customers that the TSC fix is coming.)

If your engineers feel that changing this for everyone is too invasive, maybe we could use a kernel cmdline parameter to set a flag to trust the value in the TSC adjust MSR, like the attached patch?
trust_adj_msr_patch.diff (1.89 KB)

James Cleverdon
james.cleverdon.external@eviden.com

Apr 9 2024, 12:49 AM UTC

Hi Micah,

Any news on this patch? (We're going to be selling these systems soon and would like to tell customers that the TSC fix is coming.)

Thank you,

Micah Stone
Technical Support Engineer, SUSE Customer Support
SUSE Documentation | Knowledge Base
SUSE Technical Support Handbook

ref:!00D1i0gLOd.!500Tr07g8wT:ref

ST **SUSE Technical Support**
techsupport@suse.com

Mar 26 2024, 11:01 PM UTC

Hello James,

I just wanted to give you a quick update. Our engineers have picked up the issue and are working on it currently. Thank you for bringing this to our attention and we appreciate your work and patience while we resolve this issue.

Thank you,

Micah Stone
Technical Support Engineer, SUSE Customer Support
SUSE Documentation | Knowledge Base
SUSE Technical Support Handbook

ref:!00D1i0gLOd.!500Tr07g8wT:ref

ST **SUSE Technical Support**
techsupport@suse.com

Mar 26 2024, 5:22 PM UTC

Hello James,

Thank you for linking the KB article and for uploading a supportconfig, I will get this information forwarded to our engineering team.

Regards,

ST **SUSE Technical Support**
techsupport@suse.com

Mar 25 2024, 6:33 PM UTC

Hello James,

Thank you for contacting SUSE Customer Support.

I will bring this to the attention of our engineers and we will hopefully be able to add the patch to the kernel. Thank you for bringing this to our attention.

Regards,

Micah Stone
Technical Support Engineer, SUSE Customer Support
SUSE Documentation | Knowledge Base
SUSE Technical Support Handbook

ref:!00D1i0gLOd.!500Tr07g8wT:ref

JC **James Cleverdon**
james.cleverdon.external@eviden.com

Mar 25 2024, 6:06 PM UTC

And here's Dan's original patch.
daniel_tsc_spinics_2024-02-26.patch (1.84 KB)

JC **James Cleverdon**
james.cleverdon.external@eviden.com

Mar 25 2024, 6:00 PM UTC

This minor variation on the patch might be better accepted upstream, since the kernel coding guidelines frown on multiple assignments per line.
x.diff (713 Bytes)

Download all activities as CSV

Participants

Stop watching

Mar 25 2024, 5:58 PM UTC

Last modified at
Jun 25 2024, 3:29 PM UTC

Customer reference number
MESCA5-1217

Case escalation

You may request an escalation of your case when:

- The severity of the situation has increased.
- The progress of the case has come to a halt.
- You are dissatisfied with the resolution or response.

Start escalation